CLAIMS

What is claimed is:

1. A method for manufacturing an integrated circuit comprising a plurality of semiconductor devices including an n-type transistor and a p-type transistor on a semiconductor wafer, the method comprising:

covering the p-type transistor with a mask; and

oxidizing a portion of a gate polysilicon of the n-type transistor, such that tensile mechanical stresses are formed within a channel of the n-type transistor.

2. The method of claim 1, wherein the step of covering comprises covering the p-type transistor with a mask made of nitride.

3. The method of claim 1, wherein the step of oxidation is performed using low temperature oxidation.

4. The method of claim 1, wherein the step of oxidation is performed using at least one of high pressure oxidation or atomic oxidation or plasma oxidation.

5. The method of claim 1, wherein the step of oxidation is performed between a temperature of about 25°C to about 600°C.

6. The method of claim 1, further comprising forming a planarized oxide layer on the semiconductor wafer.

7. The method of claim 6, further comprising removing silicide material from above the gate polysilicon of the n-type field effect transistor.

8. The method of claim 7, wherein the step of removing silicide material from above the gate polysilicon of the n-type field effect transistor comprises etching the silicide material from above the gate polysilicon of the n-type field effect transistor.

9. The method of claim 1, further comprising removing deposited oxide from above the gate polysilicon of the n-type field effect transistor by etching the deposited oxide from above the gate polysilicon of the n-type field effect transistor.

10. The method of claim 9, further comprising depositing silicide material on at least the portion of the gate polysilicon of the n-type field effect transistor.

11. The method of claim 10, wherein the step of depositing silicide forming material on at least the portion of the gate polysilicon of the n-type field effect transistor comprises depositing at least one of Co, HF, Mo, Ni, Pd_2, Pt, Ta, Ti, W, and Zr.

12. The method of claim 10, further comprising removing the mask used to cover the p-type field effect transistor.

13. The method of claim 1, further comprising depositing at least one of a silicide material or a nitride cap on at least the gate polysilicon of the n-type field effect transistor and removing silicide material or the nitride cap from above the gate polysilicon of the n-type field effect transistor prior to performing the step of oxidizing.

14. The method of claim 1, wherein the step of oxidizing comprises oxidizing the gate polysilicon of the n-type field effect transistor to create a stress of about 700MPa in a channel of the n-type field effect transistor.

15. The method of claim 1, wherein the step of oxidizing comprises oxidizing the gate polysilicon of the n-type field effect transistor to create tensile mechanical stresses are about 500Pa to about 1000Pa.

16. A method for manufacturing an integrated circuit comprising a plurality of semiconductor devices including an n-type field effect transistor and a p-type field effect transistor on a semiconductor wafer, the method comprising oxidizing a portion of a gate polysilicon of the n-type field effect transistor, such that tensile mechanical stresses are formed within a channel of the n-type field effect transistor, without creating additional tensile stresses in a channel of the p-type field effect transistor.

17. An integrated circuit, comprising:

a p-type transistor having a polysilicon layer; and

an n-type transistor having a polysilicon layer, wherein, after oxidation of the polysilicon layer of the n-type transistor, the polysilicon layer of the n-type transistor has an oxide edge with the shape of a vertical bird's beak.

18. The device of claim 17, wherein the vertical bird's beak has a width and height of about 20Å to about 100Å.

19. The device of claim 18, wherein the polysilicon gate has a base which is wider than an uppermost surface thereof and side edges taper towards the uppermost surface thereof.

20. The device of claim 19, wherein in a region where the polysilicon tapers towards the uppermost surface, at least a portion of the polysilicon layer and a portion of an oxide layer are present along a plane perpendicular to a plane of the base of the polysilicon.